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Description

AMPLIFYING CIRCUIT

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an amplifying circuit, and more specifically, to an amplifying circuit capable of having high equivalent input impedance, high voltage gain (or high voltage attenuation), or a large time constant.

[0003] 2. Description of the Prior Art

[0004] In basic circuit structures, amplifying circuits play a very important role. An amplifying circuit can be classified for different uses such as signal amplifying or power amplifying according to its application, the most common of which is the signal amplifying circuit.

[0005] Please refer to Fig.1 showing an example of a signal amplifying circuit using an operational amplifier. In the structure shown in Fig.1, a formula as follows can be applied. Since the negative input end of the operational amplifier is virtually grounded, the voltage on the negative

input end is 0V. Therefore, no current flows through the negative input end, and an equation $I_1+I_2=0$ can be found.As a result, the following formula can be found:

[0006] $Vo/Vi = -Z_2/Z_1$ formula 1

[0007] In general application, in order to obtain better signal quality and frequency response, an amplifying circuit having high equivalent input impedance, high voltage gain (or high voltage attenuation), or a large time constant is preferred. Thus different resistive impedances, capacitive impedances or inductive impedances are usually installed in the places of the impedance Z_1 and impedance Z_2 and arranged in different manners in order to achieve the above-mentioned objective.

[0008] However, passive elements such as resistors, capacitors and inductors used to achieve the preceding goal require very high values and therefore consume a very large circuit area when manufacturing, which causes a large cost in integrated circuit manufacturing.

SUMMARY OF INVENTION

[0009] It is therefore a primary objective of the present invention to provide an amplifying circuit.

[0010] According to an embodiment of the present invention an

amplifying circuit comprises a differential amplifier having a positive input end, a negative input end, a positive output end, a negative output end; a first input impedance coupled between the negative input end and a first input signal; a second input impedance coupled between the positive input end and the first input signal; a third input impedance coupled between the negative input end and a second input signal and being substantially the same as the second input impedance; a fourth input impedance coupled between the positive input end and the second input signal and being substantially the same as the first input impedance; a first output impedance coupled between the negative input end and the positive output end; a second output impedance coupled between the negative input end and the negative output end; a third output impedance coupled between the positive input end and the positive output end and being substantially the same as the second output impedance; and a fourth output impedance coupled between the positive input end and the negative output end and being substantially the same as the first output impedance;wherein the positive output end is for outputting a first output signal and the negative output end is for outputting a second output signal.

[0011] Also according to another embodiment of the present invention, an amplifying circuit comprises an operational amplifier having a positive input end, a negative input end, an output end; a first input impedance coupled between the negative input end and a first input signal; a second input impedance coupled between the negative input end and a second input signal; and an output impedance coupled between the negative input end and the output end;wherein the output end is for outputting an output signal.

[0012] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0013] Fig.1 illustrates an example of a signal amplifying circuit using an operational amplifier.

[0014] Fig.2 illustrates an embodiment of an amplifying circuit according to the present invention.

[0015] Fig.3 illustrates a first switched capacitor circuit.

[0016] Fig.4 illustrates an embodiment of a circuit diagram of the

switched capacitor circuit in Fig.3.

[0017] Fig.5 illustrates a second switched capacitor circuit.

[0018] Fig.6 illustrates an embodiment of a circuit diagram of the switched capacitor circuit in Fig.5.

[0019] Fig.7 illustrates another embodiment of an amplifying circuit according to the present invention.

DETAILED DESCRIPTION

[0020] Please refer to Fig.2 showing one embodiment of an amplifying circuit 10 according to the present invention. The amplifying circuit 10 comprises a differential amplifier 20, which includes a positive input end, a negative input end (shown as +, - on the left of the differential amplifier 20 in Fig.2), a positive output end, and a negative output end (shown as +, - on the right of the differential amplifier 20 in Fig.2); a first input impedance 12 coupled between the negative input end and a first input signal Vi_1; a second impedance 14 coupled between the positive input end and the first input signal Vi_1; a third input impedance 16 coupled between the negative input end and a second input signal $Vi_2$and is substantially the same as the second input impedance 14 meaning that the circuit characteristics and values of both are the same; a fourth impedance 18

coupled between the positive input end and the second input signal Vi_2 and is substantially the same as the first input impedance 12; a first output impedance 22 connected between the negative input end and the positive output end; a second output impedance 24 connected between the negative input end and the negative output end; a third output impedance 26 connected between the positive input end and the positive output end and is substantially the same as the second output impedance 24;and a fourth output impedance 28 connected between the positive input end and the negative output end and is substantially the same as the first output impedance 22. In this embodiment, the signal on the positive output end is taken as a first output signal Vo_1, and the signal on the negative output end is taken as a second output signal Vo_2.

[0021] Please note that in this embodiment, depending on the requirements on circuit design, these input impedances 12, 14, 16, 18, and these output impedance 22, 24, 26, 28 can be resistive impedances, capacitive impedances or inductive impedances.

[0022] The settings of the amplifying circuit 10 according to the present invention for high equivalent input impedance,

high voltage gain (or high voltage attenuation), and a large time constant will be described respectively as follows. In the following description, since a typical amplifying circuit operates in a differential mode, the first input signal Vi_1 is taken as an input voltage of Vi, the second input signal Vi_2 is taken as an input voltage of -Vi, the first output signal Vo_1 is taken as Vo, and the second output signal Vo_2 is taken as Vo. Moreover, it is assumed that the positive input end and the negative input end of the differential amplifier 20 are virtually grounded (i.e. 0V), and the input impedance of the differential amplifier 20 is substantially infinite (i.e. no current flows between the input ends).

[0023] If a high equivalent input impedance is desired, the first input impedance 12 and the fourth input impedance 18 are set up to be resistive impedances with a value of Ri, and the second input impedance 14 and the third input impedance 16 are set up to be resistive impedances with a value of $Ri(1+\alpha)$, wherein $|\alpha| << 1$; that is, the value of the first input impedance 12 and that of the second input impedance 14 are very close, and the value of the third input impedance 16 and that of the fourth input impedance 18 are very close. Under these settings, an

equation of current i_1 flowing through the negative input end of the differential amplifier 20 can be found as follows:

$$\frac{Vi_1 - 0}{Ri} + \frac{Vi_2 - 0}{Ri(1+\alpha)} = i_1$$

[0024] In this case, where the first input signal Vi_1 equals to Vi, the second input signal Vi_2 equals to Vi, and the current i_1 is an input current i_i, the above-mentioned equation can be derived to obtain the following result:

[0025]

$$\frac{Vi}{i_i} = \frac{Ri(1+\alpha)}{\alpha} \cong \frac{Ri}{\alpha} \qquad \because |\alpha| << 1$$

formula 2

[0026] As shown by formula 2, the ratio between the input voltage Vi and the input current i_i (i.e. equivalent input impedance) is approximately equal to Ri/α. Since the absolute value of α is far less than 1, the equivalent input impedance in Fig.2 can have a very large value in the structure of the amplifying circuit 10 according to the present invention. Please note that, the same equation will

be found on the current of the positive end of the differential amplifier 20, so a further description is hereby omitted.

[0027] If a high voltage gain is desired, the first input impedance 12 and the fourth input impedance 18 are set up to be resistive impedances with a value of Ri, the second input impedance 14 and the third input impedance 16 are set up to be substantially infinite, the first output impedance 22 and the fourth output impedance 28 are set up to be resistive impedances with a value of Rf, and the second output impedance 24 and the third output impedance 26 are set up to be resistive impedances with a value of $Rf(1+\beta)$, wherein $|\beta| << 1$; that is, the value of the first output impedance 22 and that of the second output impedance 24 are very close, and the value of the third output impedance 26 and that of the fourth output impedance 28 are very close. Under these settings, an equation of current i_1 flowing through the negative input end of the differential amplifier 20 can be found as follows:

[0028]
$$\frac{Vi_1 - 0}{Ri} = -\left(\frac{Vo_1 - 0}{Rf} + \frac{Vo_2 - 0}{Rf(1+\beta)}\right)$$

[0029] Since the first input signal Vi_1 equals to Vi, the first output signal Vo_1 equals to Vo, and the second output signal Vo_2 equals to Vo, the above-mentioned equation can be derived to obtain the following result:

[0030] $$\frac{Vo}{Vi} = -\frac{Rf}{Ri} \times \frac{1}{\beta / 1+\beta} \cong -(\frac{Rf}{Ri})(\frac{1}{\beta}) \qquad \because |\beta| << 1$$

formula 3

[0031] As shown by formula 3, the ratio between the input voltage Vi and the output voltage Vo (i.e. the voltage gain) is approximately equal to (Rf/Ri)/ β. Since the absolute value of β is far less than 1, the voltage gain in Fig.2 can have a very large value in the structure of the amplifying circuit 10 according to the present invention. Please note that the same equation will be found on the current of the positive end of the differential amplifier 20,so a further description is hereby omitted.

[0032] If a high voltage attenuation is desired, the first input impedance 12 and the fourth input impedance 18 are set up to be resistive impedances with a value of Ri, the second input impedance 14 and the third input impedance 16 are set up to be resistive impedances with a value of Ri(1+α), wherein |α| << 1; that is, the value of the first

input impedance 12 and that of the second input impedance 14 are very close, and the value of the third input impedance 16 and that of the fourth input impedance 18 are very close. The first output impedance 22 and the fourth output impedance 28 are set up to be resistive impedances with a value of Rf, and the second output impedance 24 and the third output impedance 26 are set up to be substantially infinite. Under these settings, an equation of current i_1 flowing through the negative input end of the differential amplifier 20 can be found as follows:

[0033]
$$\frac{Vi_1 - 0}{Ri} + \frac{Vi_2 - 0}{Ri(1+\alpha)} = -\left(\frac{Vo_1 - 0}{Rf}\right)$$

[0034] Since the first input signal Vi_1 equals to Vi, the second input signal Vi_2 equals to Vi, and the first output signal Vo_1 equals to Vo, the above-mentioned equation can be derived to obtain the following result:

[0035]
$$\frac{Vo}{Vi} = -\frac{Rf}{Ri} \times \frac{\alpha}{1+\alpha} \cong -\left(\frac{Rf}{Ri}\right)\alpha \qquad \because |\alpha| << 1$$

formula 4

[0036] As shown by formula 4, the ratio between the input volt-

age Vi and the output voltage Vo (i.e. the voltage gain) is approximately equal to (Rf/Ri)/ β. Since the absolute value of β is far less than 1, the voltage gain in Fig.2 can have a very small value in the structure of the amplifying circuit 10 according to the present invention; that is, the voltage attenuation can have a very large value in Fig.2. Please note that, the same equation will be found on the current of the positive end of the differential amplifier 20,so a further description is hereby omitted.

[0037] If a large time constant is desired, two applications are possible. The first application is that the first input impedance 12 and the fourth input impedance 18 are set up to be resistive impedances with a value of Ri,and the second input impedance 14 and the third input impedance 16 are set up to be resistive impedances with a value of Ri(1+α), wherein $|\alpha| << 1$; that is, the value of the first input impedance 12 and that of the second input impedance 14 are very close, and the value of the third input impedance 16 and that of the fourth input impedance 18 are very close. The first output impedance 22 and the fourth output impedance 28 are set up to be capacitive impedances with a value of 1/sC, and the second output impedance 24 and the third output impedance

26 are set up to be substantially infinite. Under these settings, an equation of current i_1 flowing through the negative input end of the differential amplifier 20 can be found as follows:

[0038]
$$\frac{Vi_1 - 0}{Ri} + \frac{Vi_2 - 0}{Ri(1+\alpha)} = -\left(\frac{Vo_1 - 0}{1/sC}\right)$$

[0039] Since the first input signal Vi_1 equals to Vi, the second input signal Vi_2 equals to Vi, and the first output signal Vo_1 equals to Vo, the above-mentioned equation can be derived to obtain the following result:

[0040]
$$\frac{Vo}{Vi} = -\frac{1/sC}{Ri} \times \frac{\alpha}{1+\alpha} \cong -\left(\frac{1}{s(RiC/\alpha)}\right) \qquad \because |\alpha| << 1$$

formula 5

[0041] As shown by formula 5, the time constant ratio is approximately equal to RiC/α. Since the absolute value of α is far less than 1, the time constant in Fig.2 can have a very large value in the structure of the amplifying circuit 10 according to the present invention. Please note that the same equation will be found on the current of the positive end of the differential amplifier 20,so a further description

is hereby omitted.

[0042] The second application is that the first input impedance 12 and the fourth input impedance 18 are set up to be capacitive impedances with a value of 1/sC, the second input impedance 14 and the third input impedance 16 are set up to be substantially infinite, the first output impedance 22 and the fourth output impedance 28 are set up to be resistive impedances with a value of Rf, and the second output impedance 24 and the third output impedance 26 are set up to be resistive impedances with a value of Rf(1+β), wherein $|\beta| << 1$; that is, the value of the first output impedance 22 and that of the second output impedance 24 are very close, and the value of the third output impedance 26 and that of the fourth output impedance 28 are very close. Under these settings, an equation of current i_1 flowing through the negative input end of the differential amplifier 20 can be found as follows:

[0043]
$$\frac{Vi_1 - 0}{1/sC} = -\left(\frac{Vo_1 - 0}{Rf} + \frac{Vo_2 - 0}{Rf(1+\beta)}\right)$$

[0044] Since the first input signal Vi_1 equals to Vi, the first output

signal Vo_1 equals to Vo, and the second output signal Vo_2 equals to Vo, the above-mentioned equation can be derived to obtain the following result:

[0045] $$\frac{Vo}{Vi} = -\frac{Rf}{1/sC} \times \frac{1}{\beta/1+\beta} \cong -s(RfC/\beta) \qquad \because |\beta| << 1$$

formula 6

[0046] As shown by formula 6, the time constant ratio is approximately equal to RiC/β. Since the absolute value of β is far less than 1, the time constant in Fig.2 can be a very large value in the structure of the amplifying circuit 10 according to the present invention. Please note that the same equation will be found on the current of the positive end of the differential amplifier 20,so a further description is hereby omitted.

[0047] In order to manufacture two resistive impedances of very close values in an IC such as the above-mentioned Ri and Ri(1+α) or Rf and Rf(1+β) so that the value of α and β can satisfy the requirements, the present invention discloses two applications using a switched capacitor circuit to implement the first input impedance 12, the second input impedance 14, the third input impedance 16, the fourth input impedance 18, the first output impedance 22, the

second output impedance 24, the third output impedance 26, or the fourth output impedance 28 as follows.

[0048] Please refer to Fig.3 showing a first switched capacitor circuit 30 according to the first application. The switched capacitor circuit 30 comprises a capacitor 32 coupled between a first node N_1 and a ground end for storing electrical charges, a first switch 34 with one of its ends coupled to the first node N1and the other end taken as an end A of the switched capacitor circuit 30, and a second switch 36 with one of its ends coupled to the first node N_1 and the other end taken as another end B of the switched capacitor circuit 30. Please note that, in actual operation, the first switch 34 and the second switch 36 are turned on alternately, and the duration of being turned on is the same.

[0049] Please refer to Fig.4 showing an embodiment of a circuit diagram of the switched capacitor circuit 30 in Fig.3. As shown in Fig.4, the first switch 34 and the second switch 36 are the same in type (e.g. both are NMOS transistors in Fig.4). The first switch 34 is controlled by a first periodical signal ψ_1, and the second switch 36 is controlled by a second periodical signal ψ_2. The active state of the first periodical signal ψ_1 and that of the second periodical sig-

nal ψ_2 are alternate, and the duty cycle of the first periodical signal ψ_1 and of the second periodical signal ψ_2 are the same. In Fig.4, since the first switch 34 and the second switch 36 are NMOS transistors, the first periodical signal ψ_1 and the second periodical signal ψ_2 are in active state when high; that is, when the periodical signal is in high voltage level, the switch being controlled is turned on.

[0050] A description to the operation of the switched capacitor circuit 30 in Fig.4 is as follows. Assume that the end A of the switched capacitor circuit 30 is coupled to an equivalent voltage source.First the first periodical signal ψ_1 is set up to be in high voltage level, and the second periodical signal ψ_2 is set up to be in low voltage level so that the first switch 34 is turned on while the second switch 36 is turned off, and a charge path is formed from the end A via the first switch 34 and the capacitor 32 to the ground end. The equivalent voltage source charges the capacitor 32 during the time the first periodical signal ψ_1 is in high voltage level (i.e. active) so that the capacitor 32 stores electrical charges. Then the second periodical signal ψ_2 is set up to be in high voltage level, and the first periodical signal ψ_1 is set up to be in low voltage level so that the

first switch 34 is turned off while the second switch 36 is turned on, and a discharge path is formed from the ground end via the capacitor 32 and the second switch 36 to the end B. The electrical charges stored in the capacitor 32 are discharged via the ground end, and a corresponding current is generated on the end B. If the frequencies of the first periodical signal ψ_1 and the second periodical signal ψ_2 are far larger than the operating frequency of the IC of the amplifying circuit 10, the switched capacitor circuit 30 can be regarded as equivalent to a resistive impedance because the end A is driven by the equivalent voltage source, and a current is consequentially generated on the end B.

[0051] In Fig.4 if taking the capacitance of the capacitor 32 as C_1, the period of the first periodical signal ψ_1 and the second periodical signal ψ_2 as T, then the impedance between the end A and the end B of the switched capacitor circuit 30 is equal to T/C_1. Therefore, to generate two impedances of very close values such as the above-mentioned Ri and $Ri(1+\alpha)$ or Rf and $Rf(1+\beta)$, only a proper control on the period of the first periodical signal ψ_1 and the second periodical signal ψ_2 of the switched capacitor circuit 30 in Fig.4 is required.

[0052] Please refer to Fig.5 showing a second switched capacitor circuit 40 according to the second application. The switched capacitor circuit 40 comprises a capacitor 42 coupled between a first node N_1 and a second node N_2 for storing electrical charges, a first switch 44 with one of its ends coupled to the first node N_1 and the other end taken as an end A of the switched capacitor circuit 40, a second switch 46 connected between the first node N_1 and a ground end, a third switch 48 with one of its ends coupled to the second node N_2 and the other end taken as another end B of the switched capacitor circuit 30, and a fourth switch 50 connected between the second node N_2 and the ground end. Please note that, in actual operation, the first switch 44 accompanied by the fourth switch 50 and the second switch 46 accompanied by the third switch 48 are turned on alternately, and the duration of being turned on is the same.

[0053] Please refer to Fig.6 showing an embodiment of a circuit diagram of the switched capacitor circuit 40 in Fig.5. As shown in Fig.6, the first switch 44, the second switch 46, the third switch 48 and the fourth switch 50 are of the same in type (e.g. all are NMOS transistors in Fig.6). The first switch 44 and the fourth switch 50 are controlled by

a first periodical signal ψ_1, and the second switch 46 and the third switch 48 are controlled by a second periodical signal ψ_2. The active state of the first periodical signal ψ_1 and that of the second periodical signal ψ_2 are alternate, and the duty cycle of the first periodical signal ψ_1 and of the second periodical signal ψ_2 are the same. In Fig.6, since the first switch 44, the second switch 46, the third switch 48 and the fourth switch 50 are NMOS transistors, the first periodical signal ψ_1 and the second periodical signal ψ_2 are in active state when high; that is, when the periodical signal is in high voltage level, the switch being controlled is turned on.

[0054] A description to the operation of the switched capacitor circuit 40 in Fig.6 is as follows. Assume that the end A of the switched capacitor circuit 40 is coupled to an equivalent voltage source.First the first periodical signal ψ_1 is set up to be in high voltage level, and the second periodical signal ψ_2 is set up to be in low voltage level, so that the first switch 44 and the fourth switch 50 are turned on while the second switch 46 and the third switch 48 are turned off, and a charge path is formed from the end A via the first switch 44, the capacitor 42, and the fourth switch 50 to the ground end. The equivalent voltage source

charges the capacitor 42 during the time the first periodical signal ψ_1 is in high voltage level (i.e. active) so that the capacitor 42 stores electrical charges. Then the second periodical signal ψ_2 is set up to be in high voltage level, and the first periodical signal ψ_1 is set up to be in low voltage level so that the first switch 44 and the fourth switch 50 are turned off while the second switch 46 and the third switch 48 are turned on, and a discharge path is formed from the ground end via the second switch 46, the capacitor 42 and the third switch 48 to the end B. The electrical charges stored in the capacitor 42 are discharged via the ground end, and a corresponding current is generated on the end B. If the frequencies of the first periodical signal ψ_1 and the second periodical signal ψ_2 are far larger than the operating frequency of the IC of the amplifying circuit 10, the switched capacitor circuit 40 can be regarded as equivalent to a resistive impedance, because the end A is driven by the equivalent voltage source and the current is consequentially generated on the end B.

[0055] In Fig.6 if taking the capacitance of the capacitor 42 as C_2, the period of the first periodical signal ψ_1 and the second periodical signal ψ_2 as T, then the impedance between the end A and the end B of the switched capacitor circuit 40 is

equal to T/C_2. Therefore, to generate two impedances of very close values such as the above-mentioned Ri and Ri(1+α) or Rf and Rf(1+β), only a proper control on the period of the first periodical signal ψ_1 and the second periodical signal ψ_2 of the switched capacitor circuit 40 in Fig.6 is required.

[0056] In addition to the configuration in differential mode as shown in Fig.2, the amplifying circuit according to the present invention can be also configured as in single-ended mode. Please refer to Fig.7 showing an amplifying circuit 60 according to a second embodiment of the present invention. The amplifying circuit 60 comprises an operational amplifier 70, which includes a positive input end, a negative input end (shown as +, - on the left of the operational amplifier 70 in Fig.7), and an output end; a first input impedance 62 coupled between the negative input end and a first input signal Vi_1; a second impedance 64 coupled between the negative input end and the second input signal Vi_2; and a first output impedance 66 connected between the negative input end and the output end. In this embodiment, the positive input end is connected to a DC voltage source (generally of 0V) for providing bias voltage, the signal on the positive output end

is taken as a first output signal Vo_1, and the signal on the negative output end is taken as a second output signal Vo_2. Please note that, the operational amplifier 70 in Fig.7 uses a differential amplifier with its positive output end (shown as + on the right of the operational amplifier 70 in Fig.7) taken as the output end of the operational amplifier 70.

[0057] Please note that in this embodiment, depending on the requirements on circuit design, the first input impedance 62, the second input impedance 64, or the first output impedance 66 can be resistive impedances, capacitive impedances or inductive impedances.

[0058] Similarly to the amplifying circuit 10 in Fig.2, through proper settings of the types and values of the first input impedance 62, the second input impedance 64 and the first output impedance 66 accompanied by formula 2, formula 4 and formula 5 mentioned above, the amplifying circuit 60 in Fig.7 is able to have high equivalent input impedance, high voltage gain (or high voltage attenuation), and large time constant. The formulas are similar to that of the amplifying circuit 10 in Fig.2; thus, a further description is hereby omitted. However please note that the first input impedance 12, the second input impedance

14 and the first output impedance 22 are replaced by the first input impedance 62, the second input impedance 64 and the first output impedance 66 in this embodiment.

[0059] Similarly, in order to manufacture two resistive impedances with very close values such as the above-mentioned Ri and Ri(1+α) or Rf and Rf(1+β), so that the value of α and β can satisfy requirements, in this embodiment the present invention can also be realized with two applications using a switched capacitor circuit to implement the first input impedance 62, the second input impedance 64, or the first output impedance 66 as the switched capacitor circuit 30 in Fig.3 and Fig.4, and the switched capacitor circuit 40 in Fig.5 and Fig.6 mentioned above. The switched capacitor circuit 30 and the switched capacitor circuit 40 applied in the amplifying circuit 60 are substantially the same to those of the earlier embodiment mentioned above, thus a further description is hereby omitted.

[0060] Please also note that for the input impedance or output impedance which is set to be substantially infinite in the various embodiments of the present invention mentioned above, one of ordinary skills in the art will be able to appreciate that such an impedance may be implemented, as

one of many different applications, by actually removing the device providing the impedance from the designated location, i.e., by creating an opened-circuit connection at the designated location.

[0061] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.